DDR3(L) SDRAM

16M x 16 Bit x 8 Banks DDR3(L) SDRAM

Feature

- **Interface and Power Supply**
  - SSTL_15: VDD/VDDQ = 1.5V(±0.075V)
  - SSTL_135: VDD/VDDQ = 1.35V(-0.067V/+0.1V)
- **JEDEC DDR3(L) Compliant**
  - 8n Prefetch Architecture
  - Differential Clock (CK/ CK) and Data Strobe (DQS/ DQS)
  - Double-data rate on DQs, DQS and DM
- **Data Integrity**
  - Auto Self Refresh (ASR) by DRAM built-in TS
  - Auto Refresh and Self Refresh Modes
- **Power Saving Mode**
  - Power Down Mode
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 ohm ± 1%)
- **Signal Synchronization**
  - Write Leveling via MR settings
  - Read Leveling via MPR
- **Programmable Functions**
  - CAS Latency (5/6/7/8/9/10/11/13)
  - CAS Write Latency (5/6/7/8/9)
  - Additive Latency (0/CL-1/CL-2)
  - Write Recovery Time (5/6/7/8/10/12/14/16)
  - Burst Type (Sequential/Interleaved)
  - Burst Length (BL8/BC4/BC4 or 8 on the fly)
  - Self Refresh Temperature Range(Normal/Extended)
  - Output Driver Impedance (34/40)
  - On-Die Termination of Rtt_Nom(20/30/40/60/120)
  - On-Die Termination of Rtt_WR(60/120)
  - Precharge Power Down (slow/fast)

Note: 1. Only Support prime DQ's feedback for each byte lane.

Ordering Information

Product ID	Max Freq.	VDD	Data Rate (CL-tRCD-tRP)	Package	Comments
CT55V128M1601 –HB	933MHz	1.35/ 1.5V	DDR3(L)-1866 (13-13-13)	96 ball BGA (7.5mmx13mm)	Pb-free
CT55V128M1601 –HL	800MHz	1.35/ 1.5V	DDR3(L)-1600 (11-11-11)		Pb-free
CT55V128M1601 –HP	933MHz	1.35/ 1.5V	DDR3(L)-1866 (13-13-13)	96 ball BGA (9mmx13mm)	Pb-free
CT55V128M1601 –HA	800MHz	1.35/ 1.5V	DDR3(L)-1600 (11-11-11)		Pb-free